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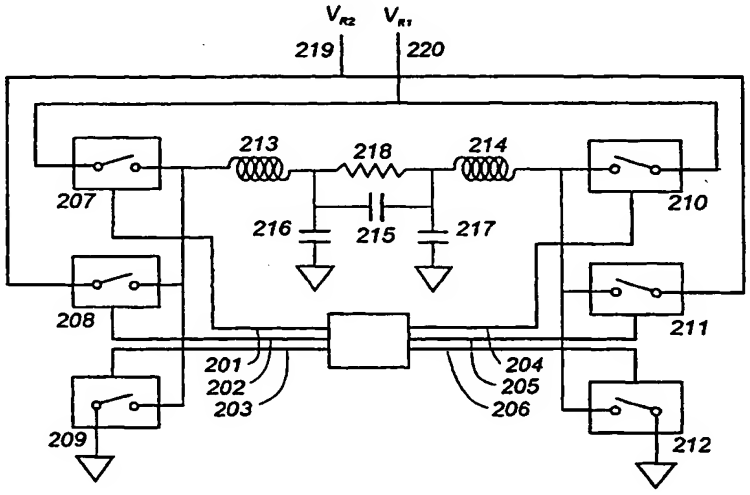
(54) Title: MULTI-REFERENCE, HIGH-ACCURACY SWITCHING AMPLIFIER



(57) Abstract: A switching amplifier employs a plurality of independent output stages in a bridged configuration, with each output stage presenting the product of an independent duty cycle and two or more static of dynamic reference voltages, currents or powers to a single terminal of a common output load. A plurality of electrically controlled switches (207, 208, 209, 210, 211, 212) interconnect the references to the load (218), with a waveform generator (220) controlling the switches for a coarse and fine control of power to the load. The waveform generator preferably uses pulse-code modulation (PCM), though the invention is not limited in this regard, and is applicable to any modulation scheme or waveform suitable to sequence the electrically controlled switches. The load is preferably filtered on either side, and return paths for the power supplies (i.e., ground) are connected through separate switches to the load through the filters (213, 214, 215, 216, 217). The amplifier may be used for audio or other applications benefitting from the design.

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(15) **Information about Correction:**
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

MULTI-REFERENCE, HIGH-ACCURACY SWITCHING AMPLIFIER

Field of the Invention

This invention relates generally to switching amplifiers and, in particular, to a switching amplifier which uses a plurality of independently referenced output stages in a bridged configuration for greater accuracy at reduced cost.

Background of the Invention

Switching amplifiers have historically relied upon the principle of modulating connection time within a fixed control period between a unipolar or bipolar power supply reference and the load. The voltage or current available to the load is essentially that of the connected power supply multiplied by the connection duty cycle (ratio of ON time to total time). An output voltage, current, or power is thus controlled in a proportional fashion by a modulating input, which is updated as frequently as once per control period. The control period typically uses ranges from 1/20th to 1/2 the period of the highest frequency of interest.

The outputs of switching amplifiers are filtered before application to the load. This reduces heterodyne products between the modulating source and the control period (aliasing). Use of shorter control periods allows use of lower-Q output filters, whereas longer control periods mandate sharp filter slopes. Filter costs therefore encourage the use of shorter control periods.

In the past decade, the dynamic range of sources for amplification has increased dramatically. A typical digital audio source now has a dynamic range of 96 dB and a bandwidth of 20 kHz. In order to accurately amplify such a signal, a typical switching amplifier output stage then requires maximum timing resolution of roughly one part in 65,000 within a 40 kHz control frequency, a resolution substantially less than one nanosecond.

Figure 1 shows a typical prior-art bridge switching amplifier output stage using a single reference for both output drivers. Figure 2 shows the timing requirements of the amplifier output stage, wherein waveforms 202-205 correspond to the (active-high) drives applied to the electrically controlled switches 102-105 in Figure 1. Power supply 101 is connected to switches 102 and 104 in order to control voltage to the load 108 through either filter 106 or 107. The return path of power supply 101 is connected to switches 103 and 105 in order to complete the path.

Control of switches 102 through 105 is effectuated by control circuit 109. Filters 106 and 107 serve to remove switching components from the output. Switches 102 and 103 are activated exclusively with a specific duty cycle, while switch 105 is activated to provide one polarity to the load 108, via filters 106 and 107. Alternatively, switches 104 and 105 are activated exclusively with a specific duty cycle, while switch 103 is activated to provide an opposite polarity to the load 108 through filters 106 and 107.

In the event that the output stage of Figure 1 is operated at a typical rate of 100 kHz, the time resolution to accurately amplify a signal with 96 dB dynamic range (one part in 65536) is seen to be the reciprocal of 100 kHz divided by 65536, or 153

picoseconds. This is beyond the capability of common-available silicon semiconductors. A different approach is indicated in order to accurately amplify high-bandwidth, high-accuracy signals at reasonable cost.

Summary of the Invention

This invention resides in a switching amplifier incorporating a plurality of independent output stages in a bridged configuration. Broadly, each output stage presents the product of an independent duty cycle and two or more static or dynamic reference voltages, currents, or powers to a single terminal of a common output load. The configuration achieves higher accuracy at lower cost than conventional designs by utilizing multiple references to produce an output voltage, current, or power with relaxed timing requirements.

In the preferred embodiment, first and second voltage references are used, with the voltage of the first reference being higher than the voltage of the second reference. The first voltage reference is higher than the second voltage reference by a factor that is a power of two. A plurality of electrically controlled switches interconnect the references to the load, and waveform generator controls the switches in a manner whereby the first voltage is applied for a coarse control of power to the load and the second voltage is applied for a fine control of power to the load. The waveform generator preferably uses pulse-code modulation (PCM), though the invention is not limited in this regard, and is applicable to any modulation scheme or waveform suitable to sequence the electrically controlled switches.

The load is preferably filtered on either side, and returns paths for the power supplies are connected through separate switches connected to the load as filtered. In an embodiment utilizing two references, a system according to the invention preferably includes a first pair of electrically controlled switches used to connect one reference to each side of the load in series, a second pair of electrically controlled switches used to connect the other reference to each side of the load in series, and a third pair of electrically controlled switches, one on either side of the load for return-path purposes. The waveform generator in this case includes sufficient outputs to control each switch as appropriate.

Brief Description of the Drawings

FIGURE 1 shows a typical bridge switching amplifier output stage using a single reference for both output drivers;

FIGURE 2 shows the timing requirements of a typical bridged switching amplifier output stage;

FIGURE 3 shows a preferred embodiment of the invention with two dynamic references per output driver; and

FIGURE 4 shows the timing requirements of the preferred embodiment illustrated in Figure 3.

Detailed Description of the Invention

This invention broadly resides in a switching amplifier incorporating two independent output stages in a bridged configuration. Each output stage presents the product of an independent duty cycle and two or more static or dynamic reference voltages, currents, or powers to a single terminal of a common output load. The configuration achieves higher accuracy at lower cost than conventional designs by utilizing multiple references to produce an output voltage, current, or power with relaxed timing requirements.

By way of an introduction, the load is connected in a bridge configuration across two (or more) independent switching amplifier output stages so as to receive the difference of their outputs; that is, the difference between two independent referenced/duty cycle products. As with existing switching amplifiers, wherein the independent duty cycle of a single reference is used for each output stage of the bridge, timing resolution limitations impact low-level modulation.

In that each output stage yields a product, it can be seen that reduction of a reference mandates an increase in duty cycle to maintain the same output. It can also be seen that reduction of a reference by any factor without commensurate duty cycle increase reduces the output of that stage by that factor.

In that the ultimate output to the load of a bridged configuration is a difference signal, it can be seen that the two output stages need not yield the same weight, or reference/duty cycle product. Coarse information of a high reference can be summed at

the load with fine information of a lower reference. Separation of coarse information from fine in a digital data stream is simply a matter of bit field selection. Analog separation is possible using differentiators.

In order to accommodate a wide dynamic range, each reference may itself be dynamic. Amplification resolution requirements are often a function of current level, as opposed to a fixed absolute. Use of dynamic references allows resolution to follow level. For example, with dynamic references, the energy applied to the load may be varied in accordance with the instantaneous value of the incoming signal, as described in U.S. Patent No. 5, 610, 553, which is incorporated herein in its entirety by reference.

By using independent references and control duty cycles for a single load, it is therefore possible to alter timing resolution requirements from those of a single switching amplifier output stage. Note that any reference changes are made appropriate to the instantaneous levels at hand in order to increase the dynamic range, and are not made solely to effect output attenuation.

Figure 3 is a diagram which illustrates a preferred embodiment of the invention incorporating two dynamic references per output driver. Figure 4 shows timing waveforms associated with the system. A first reference, VR1, is connected to switches 207 and 210 to provide energy to the load 218 through the filters on either side of the load utilizing the capacitors and inductors shown in the diagram. A second reference, VR2, supplies energy to the load 218 through the filters on either side of the load and control of the switches 208 and 211. Returns paths for the power supplies are connected through switches 209 and 212. Control of the switches is carried out by a control circuit

220, the timing diagrams for which are shown in Figure 4. The switches may be implemented using commercially available power MOSFETs or any other suitable device.

Reference VR1 is preferably higher than VR2 by a factor that is a power of two, in order to allow direct bit field extraction for the coarse/fine control. Depending upon output polarity, simultaneous switch pairs controlled are either 207/208 (coarse) with 208/209 (fine), or 210/211 (coarse) with 212/211 (fine). Control in this fashion makes VR2 a "pseudo-ground," with sinking and sourcing on opposite sides. Instantaneous differences in duty cycles are not seen by the load, in that they are substantially higher in frequency than the output filter will permit.

Signals 401-406 reflect the control signals provided through nodes 201-206. The modulation starts with decreasing coarse and fine values, then reverses sign to a coarse increase with fine decrease, followed by a coarse decrease with fine increase. Note that the numerator (active) signals are shown activated before their complements. This is done for convenience to show bit sense reversal across the differential (a "one" means sourcing on one side, but sinking on the other).

In the event that the output stage of the amplifier just described is operated at a rate of 100 kHz, for example, the timing resolution of the duty cycle required to accurately amplify a signal with 96 dB dynamic range may be derived through the reciprocal of 100 kHz, divided by 65536 and multiplied by 50, resulting in 8 nanoseconds (assuming the references exhibit the same 50:1 ratio). This is well within the capability of commercially available semiconductor devices.

I claim:

1. A switching amplifier, comprising:

a load;

first and second references, with the magnitude of the first reference being higher than the magnitude of the second reference;

a plurality of electrically controlled switches interconnecting the references to the load; and

a waveform generator controlling the switches in a manner whereby the first reference is applied for a coarse control of power to the load and the second reference is applied for a fine control of power to the load.

2. The switching amplifier of claim 1, further including a filter connected on either side of the load in series to which the switches are connected.

3. The switching amplifier of claim 1, wherein the references are voltage references.

4. The switching amplifier of claim 1, wherein the references are current references.

5. The switching amplifier of claim 1, wherein the references are power references.

6. The switching amplifier of claim 1, wherein the references are static.

7. The switching amplifier of claim 1, wherein the references are dynamic.

8. The switching amplifier of claim 1, wherein the first voltage reference is higher than the second voltage reference by a factor that is a power of two.

9. The switching amplifier of claim 1, further including an electrically controlled switch connected in series on either side of the load to ground.

10. A switching amplifier, comprising:

a load with a filter connected in series on either side;

a plurality of references, each of a different magnitude;

a plurality of electrically controlled switches interconnecting each reference to the load through both filters;

an input; and

circuitry for converting the input into a plurality of modulated signals which operate the switches for a coarse and fine control of energy to the load through the filters.

11. The switching amplifier of claim 10, wherein the references are voltage, current or power references.

12. The switching amplifier of claim 10, wherein the references are static.

13. The switching amplifier of claim 10, wherein the references are dynamic.

14. The switching amplifier of claim 10, wherein the first voltage reference is higher than the second voltage reference by a factor that is a power of two.

15. The switching amplifier of claim 10, further including an electrically controlled switch connected in series on either side of the load to ground.

16. The switching amplifier of claim 10, wherein the modulated signal is a pulse-code modulated (PCM) signal.

17. A switching amplifier, comprising:

a filtered load;

first and second voltage references, with the voltage of the first reference being higher than the voltage of the second reference;

a first pair of electrically controlled switches, one connected to each side of the filtered load in series, with the other side of each switch being connected to the first voltage reference;

a second pair of electrically controlled switches, one connected to each side of the filtered load in series, with the other side of each switch being connected to the second voltage reference;

a third pair of electrically controlled switches, one connected to each side of the filtered load in series, with the other side of each switch forming a path to ground;

a waveform generator controlling each switch in accordance with a modulated input signal.

18. The switching amplifier of claim 17, wherein the input signal is an audio signal.

19. The switching amplifier of claim 17, wherein the input signal is pulse-code modulated.

20. The switching amplifier of claim 17, wherein the waveform generator controls each switch in a manner whereby the first reference is applied for a coarse control of power to the load and the second reference is applied for a fine control of power to the load as a function of the modulated input signal.

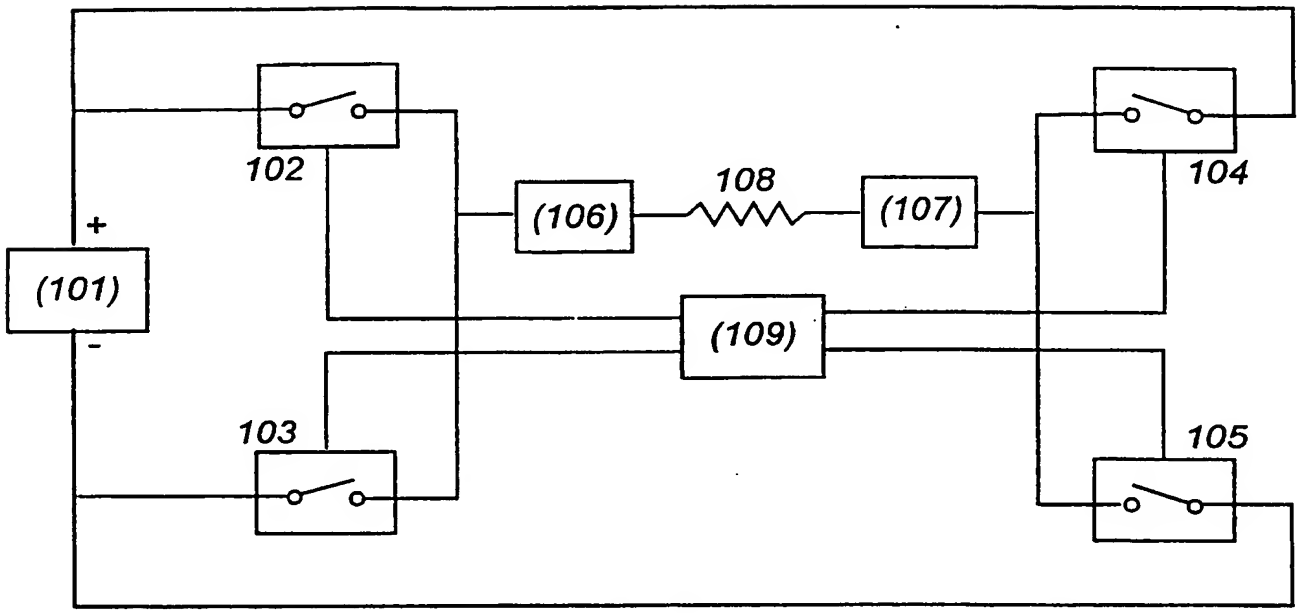

Fig - 1
(PRIOR ART)

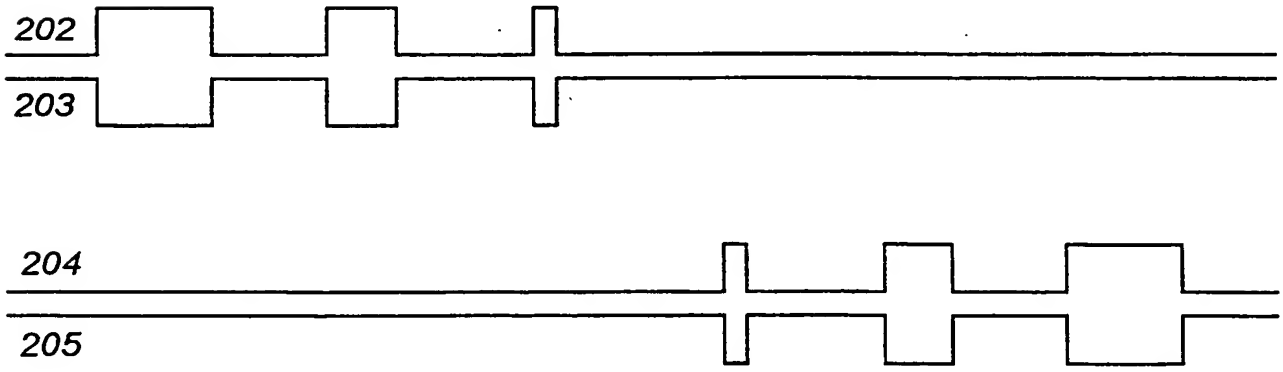

Fig - 2
(PRIOR ART)

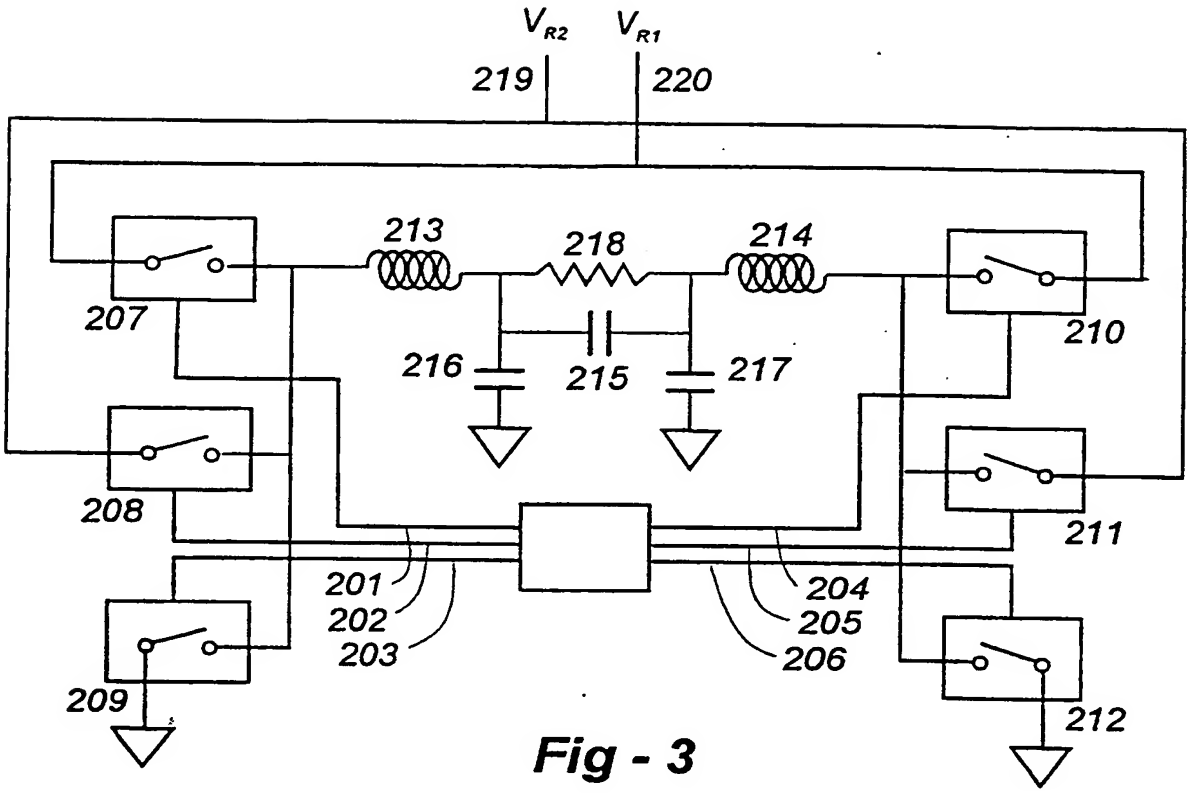

Fig - 3

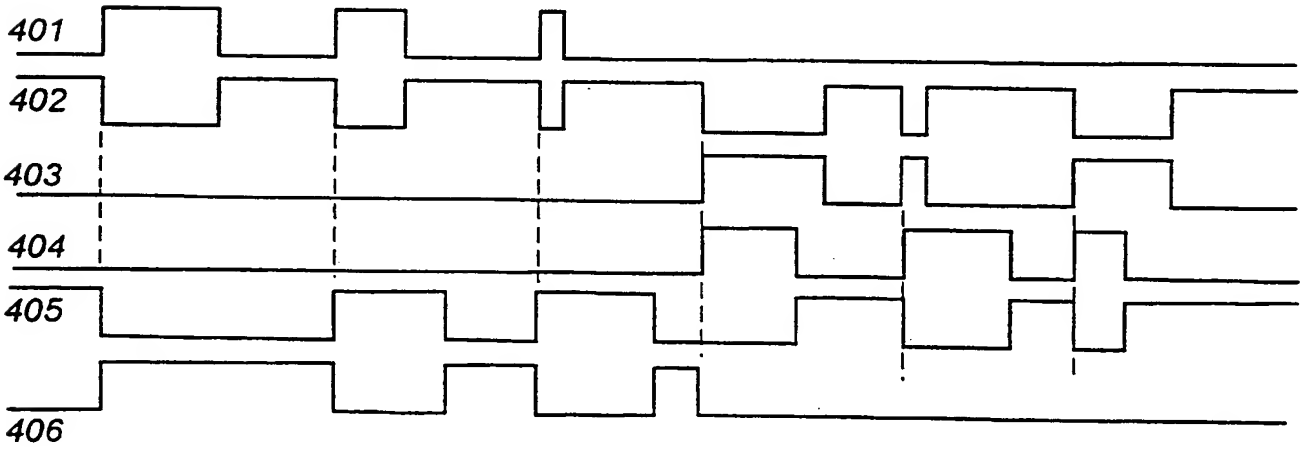

Fig - 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/26691

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H03F 3/38
US CL :330/10, 207A, 251

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 330/10, 207A, 251

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,748,421 A (SCHILLING et al.) 31 MAY 1988 (31-05-1988), figs. 4 and 6A, col. 2 line 66 to col. 3 line 55 and col. 5 lines 9-63.	1, 3-8
X	US 5,515,002 A (IDELER) 07 May 1996 (07-05-1996), fig. 2 and col. 4 line 25 to col. 5 line 13.	2, 9-16, 17-20 2,

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
15 FEBRUARY 2000	05 APR 2000

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Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/26691

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

USPTO APS WEST
search terms: switching amplifier, bridge, load, filter, coarse, fine

Form PCT/ISA/210 (extra sheet)(July 1992)★